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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2133	4

DATE MAILED: 04/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/000,089	HIRAIDE ET AL.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/04/2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-33 are presented for examination.

Priority

The examiner acknowledges the applicant's claim for a priority date of 12/7/2000 for the 1st embodiment of the invention, and 7/5/2001 for all embodiments of the invention.

Information Disclosure Statement

The examiner acknowledges consideration of the references in the applicant's Information Disclosure Statement.

Drawings

1. Figures 21 and 22 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The abstract of the disclosure is objected to because line 9 recites, "with sequential circuit elements F/Fs", but the examiner believes the meaning would be

clearer if it read, "with sequential circuit element F/Fs". Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities: page 32 line 1 recites, "Fig. 4", but the examiner believes it should read, "Fig. 23". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 6-7, 29 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Rajski et al., U.S. Patent No. 5991909.

As per Claims 1, 6 and 29:

Rajski et al. teaches a testing apparatus and method for testing an integrated circuit (column 1 lines 5-9) comprising: a pattern generator built in said integrated circuit to generate test patterns (column 4 lines 7-10 and FIG.1 12); a plurality of shift registers configured with sequential circuit elements inside said integrated circuit (column 4 lines

18-19 and FIG.1 14); and a pattern modifier (FIG.1 20 and) for modifying said test patterns generated by said pattern generator (column 3 lines 66-67 and column 4 lines 1- 3) according to an external input (FIG.1 FROM INSTRUCTION DECODER), and inputting said modified test patterns to said shift registers (FIG.1 26).

As per Claims 7 and 32:

Rajski et al. teaches the testing apparatus according to claim 1 and 29, further comprising an automatic test pattern generating unit for generating ATPG patterns (FIG.6 182) and giving said ATPG patterns as said external input to said pattern modifier (FIG.1 FROM INSTRUCTION DECODER); wherein said pattern generator generates pseudo random patterns as said test patterns (FIG.1 12); and said pattern modifier modifies said pseudo random patterns (FIG.1 LFSR) on the basis of said ATPG patterns (FIG.1 20) given from said automatic test pattern generating unit (column 5 lines 29-65).

5. Claims 2, 4 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Rajski et al., U.S. Patent No. 6557129.

As per Claims 2 and 30:

Rajski et al. teaches a testing apparatus for an integrated circuit (column 1 lines 10-15) comprising: a plurality of shift registers (FIG.9 82), to which test patterns are inputted (column 6 lines 66-67 and column 7 lines 1-2), configured with sequential circuit elements inside said integrated circuit (column 2 lines 3-7); a mask for masking an indeterminate value in outputs from said shift registers (column 4 lines 22-25 and

lines 43-47); and an output verifier for verifying output results masked by said mask (column 6 lines 54-65).

As per Claim 4:

Rajski et al. teaches the testing apparatus according to claim 2, wherein said output verifier includes a compressing means (FIG.8 48) for compressing said masked output results (FIG.8 46).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 3, 5 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajski et al., U.S. Patent No. 5991909, and further in view of Rajski et al., U.S. Patent No. 6557129.

As per Claims 3 and 31:

Rajski et al. 5991909 teaches a testing apparatus for an integrated circuit (column 1 lines 5-9) comprising: a pattern generator built in said integrated circuit to generate test patterns (column 4 lines 7-10 and FIG.1 12); a plurality of shift registers configured with sequential circuit elements inside said integrated circuit (column 4 lines 18-19 and FIG.1 14); and a pattern modifier (FIG.1 20 and) for modifying said test patterns generated by said pattern generator (column 3 lines 66-67 and column 4 lines 1- 3) according to an external input (FIG.1 FROM INSTRUCTION DECODER), and inputting said modified test patterns to said shift registers (FIG.1 26). The reference however fails to teach a masked scan chain output to a verifier. In analogous art, Rakski et al. 6557129 does teach these features. 6557129 teaches a mask for masking an indeterminate value in outputs from said shift registers (column 4 lines 22-25 and lines 43-47); and an output verifier for verifying output results masked by said mask (column 6 lines 54-65). And the reference, in column 1 lines 3-10 describes the advantage of the

device to be a better compactor which can control outputs of the scan to account for unknown states in the logic. One with ordinary skill in the art at the time of the invention, motivated as suggested by the 2nd reference, would combine the inventions, and so the claim is rejected.

As per Claim 5:

Rajski et al. 5991909 teaches the testing apparatus according to claim 3, wherein said output verifier includes a compressing means (FIG.8 48) for compressing said masked output results (FIG.8 46).

7. Claims 9, 11, 13, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajski et al., U.S. Patent No. 5991909, and further in view of Farnsworth et al., U.S. Patent No. 6708305.

As per Claims 9 and 11:

Rajski et al. teaches the testing apparatus according to claim 7, wherein said pattern modifier selects a suitable combination of one pseudo random pattern and one ATPG pattern from said pseudo random patterns generated by said pattern generator and said ATPG patterns as said external input (column 5 lines 29-65), but does not specifically teach modifying the PSRG pattern on the basis of said selected ATPG pattern. However, in an analogous art, Farnsworth et al. does teach this feature. Farnsworth et al. teaches modifying the PSRG pattern on the basis of said selected ATPG pattern (column 2 lines 33-67). And in column 2 lines 26-29, the inventor recites an advantage as being a way to perform deterministic testing without requiring the high bandwidth required by off-chip testers. And one with ordinary skill in the art at the time

of the invention, motivated as suggested by Farnsworth et al., would combine the art, and so the claims are rejected.

As per Claim 13:

Rajski et al. teaches the testing apparatus according to claim 7, but does not teach a characteristic information determining unit. However, in an analogous art, Farnsworth et al. does teach an apparatus further comprising a characteristic information determining unit for comparing said pseudo random patterns generated by said pattern generator with said ATPG patterns as said external input to determine characteristic information on said pattern generator with which said pattern generator can generate pseudo random patterns analogous to said ATPG patterns; wherein said pattern generator generates said pseudo random patterns on the basis of said characteristic information determined by said characteristic information determining unit (column 2 lines 33-67 and column 3 lines 1-17). And in column 2 lines 26-29, the inventor recites an advantage as being a way to perform deterministic testing without requiring the high bandwidth required by off-chip testers. And one with ordinary skill in the art at the time of the invention, motivated as suggested by Farnsworth et al., would combine the art, and so the claim is rejected.

As per Claim 15:

Rajski et al. and Farnsworth et al. teach the testing apparatus according to claim 13, and additionally wherein said characteristic information is a seed value to be set to said pattern generator (Farnsworth et al. column 4 lines 50-59). And, in view of the previously recited motivation for Farnsworth et al., the claim is rejected.

As per Claims 17:

Rajski et al. and Farnsworth et al. teach the testing apparatus according to claim 13, wherein said pattern generator is configured as a linear feedback shift register (Rajski et al., FIG.1 12), and said characteristic information (Rajski et al. FIG.1 FROM INSTRUCTION DECODER) is a feedback position in said linear feedback shift register (Rajski et al. FIG.1 20). And in view of the previously recited motivation for Farnsworth et al., the claim is rejected.

8. Claims 8, 20, 22, 24, 26 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajski et al., U.S. Patent No. 5991909, and further in view of Rajski et al., U.S. Patent No. 6557129, and further in view of Rajski et al., U.S. Patent No. 6327687.

As per Claims 8 and 33:

Rajski et al. 5991909 and 6557129 teach the testing apparatus according to claim 3 and 31, but fails to specify the ATPG applications of the subject claims. However, in an analogous art, Rajski et al. 6327687 does teach this feature. Rajski et al. 6327687 teaches the apparatus further comprising an automatic test pattern generating unit for generating ATPG patterns and giving said ATPG patterns as said external input to said pattern modifier (column 4 lines 55-67); wherein said pattern generator generates pseudo random patterns as said test patterns; and said pattern modifier modifies said pseudo random patterns on the basis of said ATPG patterns given from said automatic test pattern generating unit (column 5 lines 1-20). And column 4 lines 25-33 explains that an advantage needed in the art is the ability to seed

an LFSR quickly in order to better utilize tester time. And one with ordinary skill in the art at the time of the invention, motivated by the aforementioned advantage, would combine the references, and so the claims are rejected.

As per Claim 20:

Rajski et al., 5991909 teaches the testing apparatus according to claim 8, but fails to teach any limitations to the compression process. But in an analogous art, Rajski et al., 6327687 does teach the feature; further comprising an execution limitation condition setting unit for setting, when said automatic test pattern generating unit executes a compressing process on said ATPG pattern, an execution limitation condition for limiting the execution of said compressing process; wherein said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when said execution limitation condition set by said execution limitation condition setting unit is satisfied (column 14 lines 45-67 and column 15 lines 1-8). And column 4 lines 25-33 explains that an advantage needed in the art is the ability to seed an LFSR quickly in order to better utilize tester time. And one with ordinary skill in the art at the time of the invention, motivated by the aforementioned advantage, would combine the references, and so the claim is rejected.

As per Claim 22:

Both Rajski et al. references teach the testing apparatus according to claim 20, wherein said execution limitation condition setting unit sets, as said execution limitation condition, an upper limit value of the number of faults to be detected with one ATPG pattern, and said automatic test pattern generating unit terminates said

compressing process on said ATPG pattern when the number of detection target faults, that are compressed in said ATPG pattern by said compressing process, reaches said upper limit value (Rajski et al. 6327687 column 14 lines 65-68). And in view of the motivation cited previously, the claim is rejected.

As per Claim 24:

Both Rajski et al. references teach the testing apparatus according to claim 22, the testing apparatus according to claim 22, wherein said execution limitation condition setting unit increases said upper limit value as generation of said ATPG pattern progresses (Rajski et al. 6327687 column 14 lines 30-44). And in view of the motivation cited previously, the claim is rejected. .

As per Claim 26:

Both Rajski et al. references teach the testing apparatus according to claim 20, the testing apparatus according to claim 20, wherein said execution limitation condition setting unit sets, as said execution limitation condition, an upper value of a quantity of pattern modification by said pattern modifier in the case where said pattern modifier modifies one of said pseudo random patterns on the basis of one ATPG pattern, and said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when a quantity of pattern modification, performed by said pattern modifier in the case where said pattern modifier modifies said pseudo random pattern on the basis of one ATPG pattern in which detection target faults are compressed by said compressing process, reaches said upper limit value (Rajski et al. 6327687

column 14 lines 30-67 and column 15 lines 1-8). And in view of the motivation cited previously, the claim is rejected.

As per Claim 28:

Both Rajski et al. references teach the testing apparatus according to claim 26, wherein said execution limitation condition setting unit increases said upper limit value as generation of said ATPG pattern progresses (Rajski et al. 6327687 column 14 lines 30-44). And in view of the motivation cited previously, the claim is rejected.

9. Claims 19, 21 23, 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajski et al., U.S. Patent No. 5991909, and further in view of Rajski et al., U.S. Patent No. 6327687.

As per Claim 19:

Rajski et al., 5991909 teaches the testing apparatus according to claim 7, but fails to teach any limitations to the compression process. But in an analogous art, Rajski et al., 6327687 does teach the feature; further comprising an execution limitation condition setting unit for setting, when said automatic test pattern generating unit executes a compressing process on said ATPG pattern, an execution limitation condition for limiting the execution of said compressing process; wherein said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when said execution limitation condition set by said execution limitation condition setting unit is satisfied (column 14 lines 45-67 and column 15 lines 1-8). And column 4 lines 25-33 explains that an advantage needed in the art is the ability to seed an LFSR quickly in order to better utilize tester time. And one with ordinary skill in the art at the time of the

invention, motivated by the aforementioned advantage, would combine the references, and so the claim is rejected.

As per Claim 21:

The Rajski et al. 5991909 reference teaches the testing apparatus according to claim 19, wherein said execution limitation condition setting unit sets, as said execution limitation condition, an upper limit value of the number of faults to be detected with one ATPG pattern, and said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when the number of detection target faults, that are compressed in said ATPG pattern by said compressing process, reaches said upper limit value (Rajski et al. 6327687 column 14 lines 65-68). And in view of the motivation cited previously, the claim is rejected.

As per Claims 23:

The Rajski et al. 5991909 reference teaches the testing apparatus according to claim 21, the testing apparatus according to claim 21, wherein said execution limitation condition setting unit increases said upper limit value as generation of said ATPG pattern progresses (Rajski et al. 6327687 column 14 lines 30-44). And in view of the motivation cited previously, the claim is rejected. .

As per Claim 25:

The Rajski et al. 5991909 reference teaches the testing apparatus according to claim 19, the testing apparatus according to claim 19, wherein said execution limitation condition setting unit sets, as said execution limitation condition, an upper value of a quantity of pattern modification by said pattern modifier in the case where said pattern

modifier modifies one of said pseudo random patterns on the basis of one ATPG pattern, and said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when a quantity of pattern modification, performed by said pattern modifier in the case where said pattern modifier modifies said pseudo random pattern on the basis of one ATPG pattern in which detection target faults are compressed by said compressing process, reaches said upper limit value (Rajski et al. 6327687 column 14 lines 30-67 and column 15 lines 1-8). And in view of the motivation cited previously, the claim is rejected.

As per Claim 27:

The Rajski et al. 5991909 reference teaches the testing apparatus according to claim 25, wherein said execution limitation condition setting unit increases said upper limit value as generation of said ATPG pattern progresses (Rajski et al. 6327687 column 14 lines 30-44). And in view of the motivation cited previously, the claim is rejected.

10. Claims 10, 12, 14, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajski et al., U.S. Patent No. 5991909, in view of Rajski et al., U.S. Patent No. 6557129, and further in view of Rajski et al., U.S. Patent No. 6327687 as applied to Claim 8 above, and further in view of Farnsworth et al., U.S. Patent No. 6708305.

As per Claims 10 and 12:

Rajski et al. teaches the testing apparatus according to claim 8, wherein said pattern modifier selects a suitable combination of one pseudo random pattern and one

ATPG pattern from said pseudo random patterns generated by said pattern generator and said ATPG patterns as said external input (column 5 lines 29-65), but does not specifically teach modifying the PSRG pattern on the basis of said selected ATPG pattern. However, in an analogous art, Farnsworth et al. does teach this feature. Farnsworth et al. teaches modifying the PSRG pattern on the basis of said selected ATPG pattern (column 2 lines 33-67). And in column 2 lines 26-29, the inventor recites an advantage as being a way to perform deterministic testing without requiring the high bandwidth required by off-chip testers. And one with ordinary skill in the art at the time of the invention, motivated as suggested by Farnsworth et al., would combine the art, and so the claims are rejected.

As per Claim 14:

Rajski et al. teaches the testing apparatus according to claim 8, but does not teach a characteristic information determining unit. However, in an analogous art, Farnsworth et al. does teach an apparatus further comprising a characteristic information determining unit for comparing said pseudo random patterns generated by said pattern generator with said ATPG patterns as said external input to determine characteristic information on said pattern generator with which said pattern generator can generate pseudo random patterns analogous to said ATPG patterns; wherein said pattern generator generates said pseudo random patterns on the basis of said characteristic information determined by said characteristic information determining unit (column 2 lines 33-67 and column 3 lines 1-17). And in column 2 lines 26-29, the inventor recites an advantage as being a way to perform deterministic testing without

requiring the high bandwidth required by off-chip testers. And one with ordinary skill in the art at the time of the invention, motivated as suggested by Farnsworth et al., would combine the art, and so the claim is rejected.

As per Claim 16:

Rajski et al. and Farnsworth et al. teach the testing apparatus according to claim 14, and additionally wherein said characteristic information is a seed value to be set to said pattern generator (Farnsworth et al. column 4 lines 50-59). And, in view of the previously recited motivation for Farnsworth et al., the claim is rejected.

As per Claims 18:

Rajski et al. and Farnsworth et al. teach the testing apparatus according to claim 14, wherein said pattern generator is configured as a linear feedback shift register (Rajski et al., FIG.1 12), and said characteristic information (Rajski et al. FIG.1 FROM INSTRUCTION DECODER) is a feedback position in said linear feedback shift register (Rajski et al. FIG.1 20). And in view of the previously recited motivation for Farnsworth et al., the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

Albert DeCady
Primary Examiner